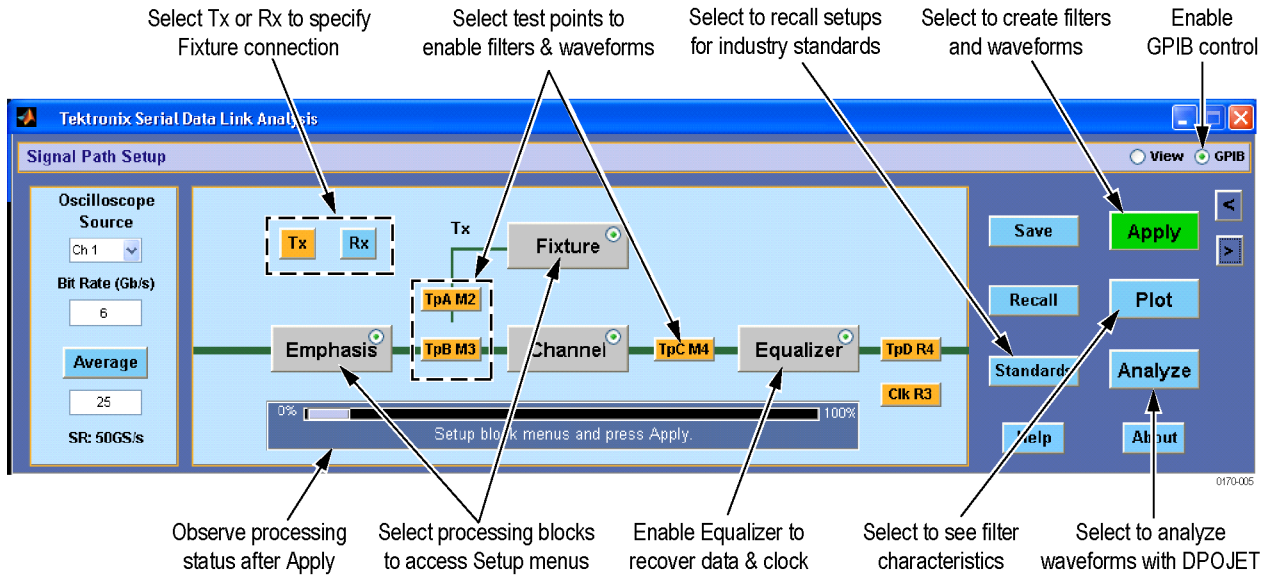# SDLA Software Reference

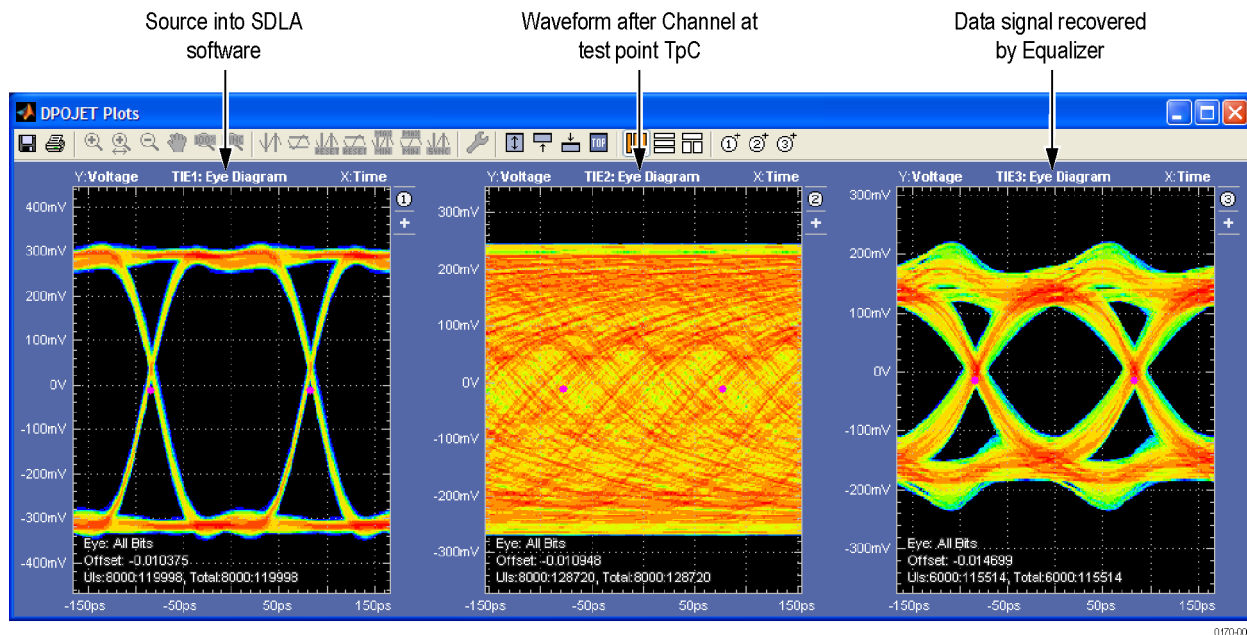**Getting Started with SDLA Software**

The SDLA Serial Data Link Analysis software helps you analyze and test your complete serial data link design for the highest speed serial data industry standards.

NOTE. *For complete operating instructions and general safety information, refer to the online help or the printable help for the application.*

The following figure shows the main SDLA Signal Path window.

Tektronix

This figure shows the DPOJET plots of three waveforms: the SDLA Source, the waveform TpC after the Channel, and the TpD waveform after the Equalizer.

Source into SDLA software

Waveform after Channel at test point TpC

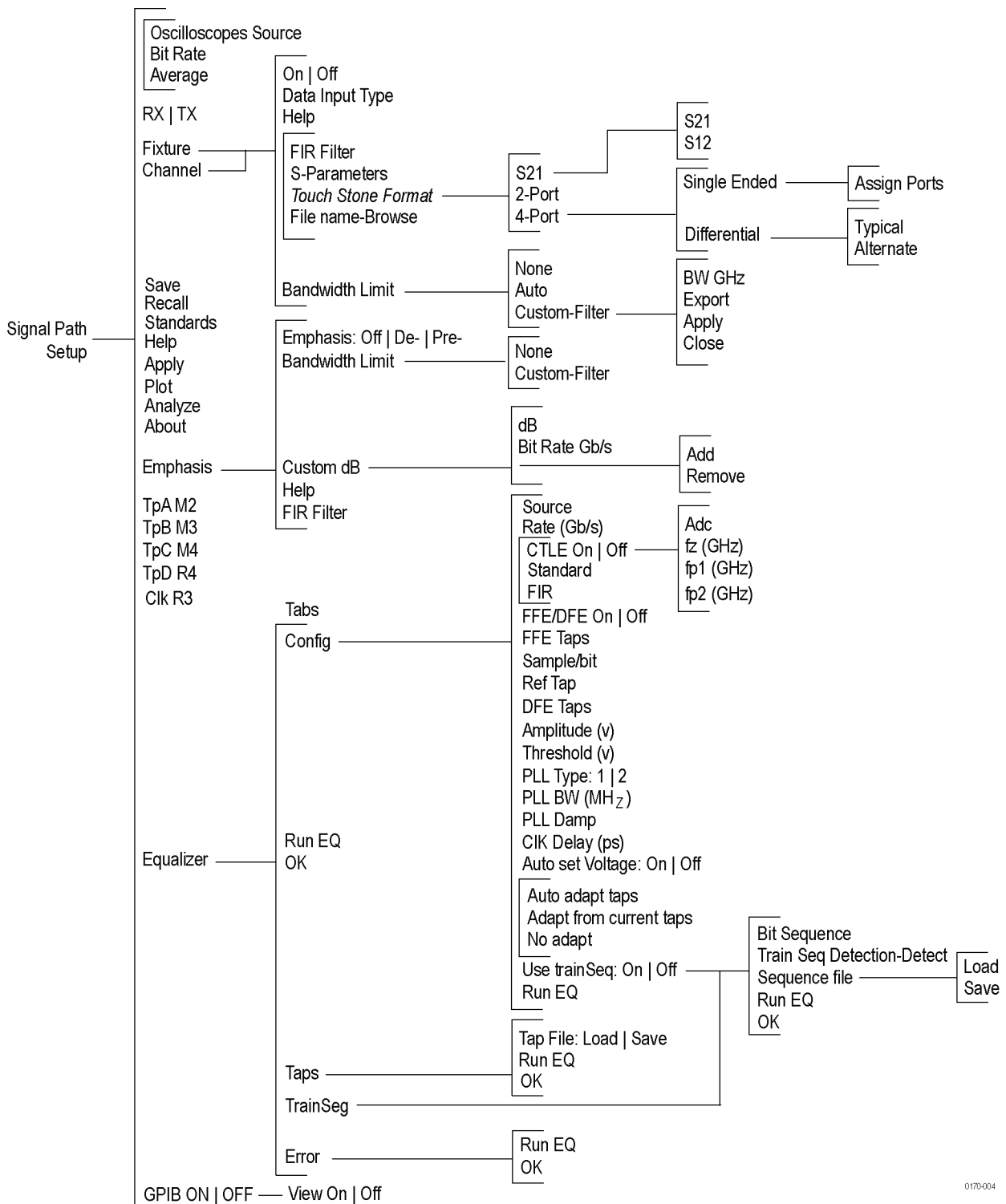Data signal recovered by Equalizer

0170-006

For up-to-date information on Tektronix oscilloscope solutions for Serial Data Link Analysis, access the www.tektronix.com/Measurement/scopes Web page.

SDLA Ordering Information

This software runs on Tektronix DPO/DSA70000 Series and Tektronix DPO/DSA70000B Series oscilloscopes. Refer to the *Optional Applications Software on Windows-Based Oscilloscopes Installation Manual* for a complete list of supported models and software requirements.

- Option SLA: SDLA Advanced – Advanced data link analysis functions including equalization

- Option SLE: SDLA Essentials – Serial Data Link Analysis Software without equalization

- Option EQ: SDLA software upgrade from Option SLE to Option SLA

SDLA Menu Tree

Oscilloscopes Source
Bit Rate
Average

RX | TX

Fixture
Channel

On | Off
Data Input Type
Help

FIR Filter
S-Parameters
Touch Stone Format
File name-Browse

S21
2-Port
4-Port

S21
S12

Single Ended — Assign Ports

Differential — Typical
Alternate

Signal Path
Setup

Save
Recall
Standards
Help
Apply
Plot
Analyze
About

Emphasis

TpA M2
TpB M3
TpC M4
TpD R4
Clk R3

Bandwidth Limit

None
Auto
Custom-Filter

BW GHz
Export
Apply
Close

Emphasis: Off | De- | Pre-
Bandwidth Limit

None
Custom-Filter

Custom dB
Help
FIR Filter

dB
Bit Rate Gb/s

Add
Remove

Source
Rate (Gb/s)
CTLE On | Off
Standard
FIR
FFE/DFE On | Off
FFE Taps
Sample/bit
Ref Tap
DFE Taps
Amplitude (v)
Threshold (v)
PLL Type: 1 | 2
PLL BW (MH$_Z$)
PLL Damp
Clk Delay (ps)
Auto set Voltage: On | Off

Adc
fz (GHz)
fp1 (GHz)
fp2 (GHz)

Tabs

Config

Run EQ
OK

Equalizer

Auto adapt taps
Adapt from current taps
No adapt

Use trainSeq: On | Off
Run EQ

Bit Sequence
Train Seq Detection-Detect
Sequence file
Run EQ
OK

Load
Save

Tap File: Load | Save
Run EQ
OK

Taps

TrainSeg

Error

Run EQ
OK

GPIB ON | OFF — View On | Off

0170-004